Amendments to the Claims:

The following claims will replace all prior versions of the claims in this application (in the unlikely event that no claims follow herein, the previously pending claims will remain):

1. (Currently Amended) A turbo code encoder comprising:

a first convolutional encoder for receiving N bits to be encoded, generating ~~a~~ N systematic bits and ~~a~~ N first parity bits, and outputting them;

an interleaver for receiving the N bits to be encoded, in parallel with the first convolutional encoder, and interleaving the N received bits;

a second convolutional encoder for receiving the N interleaved bits from the interleaver and generating ~~a~~ N second parity bits; and

a repeater for repeatedly outputting predefined bits among the 3N total bits output from the first and second convolution encoders.

2. (Original) The turbo code encoder as claimed in claim 1, wherein the repeater repeatedly outputs the systematic bit.

3. (Original) The turbo code encoder as claimed in claim 2, wherein the repeater outputs signals in the order of the systematic bit, the first parity bit, the systematic bit, and the second parity bit.

4. (Original) The turbo code encoder as claimed in claim 1, wherein the repeater repeatedly outputs the first parity bit.

5. (Original) The turbo code encoder as claimed in claim 1, wherein the repeater repeatedly outputs the second parity bit.

6. (Currently Amended) A code rate decreasing method of a turbo code encoder, comprising:

(a) receiving N bits to be encoded, and generating ~~a~~ N systematic bits and ~~a~~ N first parity bits;

(b) receiving the N bits to be encoded, and interleaving the N received bits;

(c) receiving the N interleaved bits and generating ~~a~~ N second parity bits; and

(d) repeatedly outputting predefined bits among the 3N bits output from the steps (a) and (c).

7. (Original) The code rate decreasing method as claimed in claim 6, wherein the step (d) comprises repeating the systematic bit and outputting data in the order of the systematic bit, the first parity bit, the systematic bit, and the second parity bit.

8. (Original) The code rate decreasing method as claimed in claim 6, wherein the step (d) comprises repeatedly outputting the first parity bit among the bits output from the steps (a) and (c).

9. (Original) The code rate decreasing method as claimed in claim 6, wherein the step (d) comprises repeatedly outputting the systematic bit and the first parity bit and reducing the code rate through puncturing, when the code rate is less than 1/4.

10. (New) A turbo code encoder comprising:

a first convolutional encoder for receiving N bits to be encoded, generating N systematic bits and N first parity bits, and outputting them;

an interleaver for receiving the N bits to be encoded, in parallel with the first convolutional encoder, and interleaving the N received bits;

a second convolutional encoder for receiving the N interleaved bits from the interleaver and generating ~~a~~ N second parity bits; and

a repeater for repeatedly outputting 4N predefined bits among the 3N total bits output from the first and second convolution encoders.

11. (New) The turbo code encoder as claimed in claim 10, wherein the repeater repeatedly outputs the systematic bit.

12. (New) The turbo code encoder as claimed in claim 11, wherein the repeater outputs signals in the order of the systematic bit, the first parity bit, the systematic bit, and the second parity bit.

13. (New) The turbo code encoder as claimed in claim 10, wherein the repeater repeatedly outputs the first parity bit.

14. (New) The turbo code encoder as claimed in claim 10, wherein the repeater repeatedly outputs the second parity bit.